REMARKS

The Applicants' thank the Examiner for granting a telephone interview on January 21, 2002.

Responsive to the Final Office Action of October 24, 2002, reconsideration of the above application is respectfully requested.

1. Claim rejections under 35 USC 112:

Claims 1, 2-4, 6-15, 17-19, and 21-32 have been amended to overcome rejections under 35 USC 112.

2. Claim rejections under 35 USC 102:

Independent claims 1, 16, and 31 were rejected under 35 USC 102 as being anticipated by Jiang et al. (US. 5,914,973) hereinafter referred to as the '973 patent.

Specifically, the Examiner contends that the '973 patent discloses a first and a second heat spreading layer, and the first and the second heat spreading layers allowing heat generated in the VCSEL to bypass the first and the second reflecting surfaces.

The Applicants' respectfully point out the '973 patent discloses a heat dissipation layer 30 (FIG. 1) and 54 (FIG. 3) that is **not** within the VCSEL cavity where the heat is generated but rather is on the opposite side of one of the mirrors **away** from the cavity. Furthermore, the VCSEL structure of FIG. 3 requires a mirror 54 with good thermal properties since it is located adjacent the region 21 where substantial heat is generated. Moreover, the '973 discloses the following two step process for fabricating the final VCSEL structure of FIG. 3: (i) the heat dissipation layer 30 is first formed on top of the semi-VCSEL structure (FIG. 1), and (ii) the semi-VCSEL structure is then flip-bonded to another substrate 42 (FIG. 2), having a heat dissipation layer 44 (FIG. 2), to yield a final VCSEL structure (FIG. 3) in which the heat dissipation layer is between the substrate and the mirror.

In contrast, the present invention according to amended claims 1, 16, and 31, includes at least one heat spreading layer formed between a mirror and the active layer of the VCSEL. Furthermore, this intracavity and lattice matched heat spreading layer precludes the need for reflecting mirrors with good thermal properties since the heat generated intracavity is bypassed via the heat spreading layer adjacent the active layer. Moreover, the VCSEL structure, according to the present invention, is grown in one epitaxial step on a single substrate and without the need

for flip-bonding, in contrast to the two-step/two-substrate/flip-bonding approach of the '973 patent.

Accordingly, claims 1, 16, and 31 have been amended to overcome these rejections.

In view of the above, it is submitted that this application is now in good order for allowance, and such early action is respectfully solicited. Should matters remain which the Examiner believes could be resolved in a telephone interview, the Examiner is requested to telephone the Applicants' undersigned attorney.

Respectfully submitted,

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ADDENDUM PAGES

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IN THE CLAIMS

1. (Amended) A method for reducing the temperature in a vertical-cavity surface-emitting laser (VCSEL), the method comprising:

forming at least one heat spreading layer between an active layer and at least one reflecting surface in a VCSEL; and

[forming at least one of a heat spreading layers adjacent at least one of a reflecting surfaces in a VCSEL;]

permitting for reduction of the VCSEL temperature by allowing heat to bypass the at least one reflecting surface and pass through the at least one heat spreading layer

[said at least one of the heat spreading layers reducing the VCSEL temperature by allowing heat to bypass said one of the reflecting surfaces].

2. (Amended) The method according to claim 1, including doping the at least one of the heat spreading layers with an n-type material [is doped with an n-type material].

3. (Amended) The method according to claim 2, wherein the doping with the n-type material is effected by an InP compound [the n-type material includes an InP compound].

4. (Amended) The method according to claim 1, further including forming a Distributed Bragg Reflector (DBR) as part of the at least one reflecting surface [wherein at least one of the reflecting surfaces is a Distributed Bragg Reflector (DBR)].

5. The method according to claim 1, further comprising the step of forming a tunnel junction between an apertured active region and the at least one of the reflecting surfaces.

6. (Amended) The method according to claim 5, further including having an alloy of InAlGaAs, in the active region, substantially lattice matched to InP [wherein the active region comprises an alloy of InAlGaAs approximately lattice matched to InP].

7. (Amended) The method according to claim 5, further including having an alloy of InGaAsP, in the active region, substantially lattice matched to InP [wherein the active region comprises an alloy of InGaAsP approximately lattice matched to InP].

8. (Amended) The method according to claim 5, further including an alloy of InGaAs, in the active region, substantially lattice matched to InP [wherein the active region comprises an alloy of InGaAs approximately lattice matched to InP].

9. (Amended) The method according to claim 4, further including alternating layers of $Al_{a1}Ga_{1-a1}As_bSb_{1-b}$ and $Al_{a2}Ga_{1-a2}As_bSb_{1-b}$ in the DBR [wherein the DBR is made of alternating layers of $Al_{a1}Ga_{1-a1}As_bSb_{1-b}$ and $Al_{a2}Ga_{1-a2}As_bSb_{1-b}$].

10. (Amended) The method according to claim 9, further including the step of assigning b greater than about 0.5, a1 greater than about 0.9, and a2 less than about 0.3 [wherein b is greater than about 0.5, a1 is greater than about 0.9, and a2 is less than about 0.3].

11. (Amended) The method according to claim 4, further including having an undoped DBR [wherein the DBR is undoped].

12. (Amended) The method according to claim 1, further effecting the VCSEL to exhibit continuous wave operation at temperatures greater than about 80 degrees Celsius [wherein the VCSEL exhibits continuous wave operation at temperatures greater than about 80 degrees Celsius].

13. (Amended) The method according to claim 5, further including an n-type InP and p-type InAlAs in the tunnel junction [wherein the tunnel junction comprises of n-type InP and p-type InAlAs].

14. (Amended) The method according to claim 1, further providing a thickness of about 1-3λ to the at least one heat spreading layer [wherein the heat spreading layer has a thickness of about 1-3λ].

15. (Amended) The method according to claim 5, further providing a mixture to selectively etch the active region to form an aperture in the VCSEL and simultaneously preclude substantial etching of the at least one heat spreading layer [wherein a mixture selectively etches the active region to form an aperture in the VCSEL, said mixture precluding substantial etching of the heat spreading layer].

16. (Amended) A method for reducing the thermal impedance in a vertical-cavity surface-emitting laser (VCSEL) , the method comprising:

forming a first heat spreading layer between a first reflecting surface and an active [region] layer in a VCSEL;

[providing] forming a second heat spreading layer between a second reflecting surface and the active [region] layer in a VCSEL: and

said first and second heat spreading layers reduce the thermal impedance in the VCSEL by allowing an injected current to bypass the reflecting surfaces.

17. (Amended) The method according to claim 16, wherein the forming steps include doping the heat spreading layers with an n-type material [wherein the first and the second heat spreading layers are doped with an n-type material].

18. (Amended) The method according to claim 17, including effecting the doping with the n-type material with an InP compound [wherein the n-type material includes an InP compound].

19. (Amended) The method according to claim 16, further including forming a Distributed Bragg Reflectors (DBRs) as part of the first and the second reflecting surfaces [wherein the first and the second reflecting surfaces are Distributed Bragg Reflectors (DBRs)].

20. The method according to claim 16, further comprising the step of forming a tunnel junction between an apertured active region and the first reflecting surface.

21. (Amended) The method according to claim 20, further including having an alloy of InAlGaAs, in the active region, substantially lattice matched to InP [wherein the active region comprises of an alloy of InAlGaAs approximately lattice matched to InP].

22. (Amended) The method according to claim 20, further including having an alloy of InGaAsP, in the active region, substantially lattice matched to InP [wherein the active region comprises an alloy of InGaAsP approximately lattice matched to InP].

23. (Amended) The method according to claim 20, further including having an alloy of InGaAs, in the active region, substantially lattice matched to InP [wherein the active region comprises an alloy of InGaAs approximately lattice matched to InP].

24. (Amended) The method according to claim 19 [17], further including alternating layers of $Al_{a1}Ga_{1-a1}As_bSb_{1-b}$ and $Al_{a2}Ga_{1-a2}As_bSb_{1-b}$ in the DBR [wherein the DBR is made of alternating layers of $Al_{a1}Ga_{1-a1}As_bSb_{1-b}$ and $Al_{a2}Ga_{1-a2}As_bSb_{1-b}$].

25. (Amended) The method according to claim 24 [20], further including the step of assigning b greater than about 0.5, a1 greater than about 0.9, and a2 less than about 0.3 [wherein b is greater than about 0.5, a1 is greater than about 0.9, and a2 is less than about 0.3].

26. (Amended) The method according to claim 19, further including having undoped DBRs [wherein the DBRs are undoped].

27 [23]. (Amended) The method according to claim 16, further effecting the VCSEL to exhibit continuous wave operation at temperatures greater than about 80 degrees Celsius [wherein the VCSEL exhibits continuous wave operation at temperatures greater than about 80 degrees Celsius].

28 [27]. (Amended) The method according to claim 20, further including an n-type InP and p-type InAlAs in the tunnel junction [wherein the tunnel junction comprises of n-type InP and p-type InAlAs].

29 [28]. (Amended) The method according to claim 16, further providing a thickness of about 1-3λ to each of the heat spreading layers [wherein the heat spreading layers have a thickness of about 1-3λ].

30 [29]. (Amended) The method according to claim 20, further providing a mixture to selectively etch the active region to form an aperture in the VCSEL and simultaneously preclude substantial etching of each of the heat spreading layers [wherein a mixture selectively etches the active region to form an aperture in the VCSEL, said mixture precluding substantial etching of the heat spreading layer].

31 [30]. (Amended) A vertical-cavity surface-emitting laser (VCSEL) operating at a reduced temperature, the VCSEL comprising:

a first and a second reflecting surface in a VCSEL;

[at least one active region] an active layer in the VCSEL;

a first and a second heat spreading layer in the VCSEL, said first heat spreading layer being in between the first reflecting surface and the active layer, and the second heat spreading layer being in between the second reflecting surface and the active layer; and

the first and second heat spreading layers allowing heat generated in the VCSEL to bypass the first and second reflecting surfaces, thereby reducing the temperature of the VCSEL.

32 [31]. (Amended) The vertical-cavity surface-emitting laser (VCSEL) according to claim 31 [30], wherein optical reflections at edges of the first and second heat spreading layers add in phase with optical reflections from the first and second reflecting surfaces [wherein the first and second heat spreading layers are chosen such that optical reflections from their edges add in phase with reflections from the first and second reflecting surface].

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